RECEIVED
CENTRAL FAX CENTER

APR 14 2006

PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission: 18

Application Number	10/003,170
Filing Date	November 14, 2001
First Named Inventor	Eugene Matter
Art Unit	2187
Examiner Name	Mclean-Mayo, K.
Attorney Docket Number	042390.P12396

ENCLOSURES *(Check all that apply)*

- [✓] Fee Transmittal Form
- [✓] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation
- [ ] Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [✓] Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) (please identify below):

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Intel Corporation		
Signature			
Printed name	Stuart A. Whittington		
Date	April 14, 2006	Reg. No.	45,215

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature			
Typed or printed name	Stuart A. Whittington	Date	April 14, 2006

RECEIVED
CENTRAL FAX CENTER

APR 14 2006

PTO/SB/17 (01-06)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($)

Complete if Known	
Application Number	10/003,170
Filing Date	November 14, 2001
First Named Inventor	Eugene Matter
Examiner Name	Mclean-Mayo, K.
Art Unit	2187
Attorney Docket No.	042390.P12396

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☒ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 50-0221 Deposit Account Name: Intel Corporation

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☑ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☐ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION (All the fees below are due upon filing or may be subject to a surcharge.)

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____ x	_____ =	_____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____ x	_____ =	_____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ / 50 =	_____ (round up to a whole number) x	_____ =	_____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Brief in Support of Appeal; Fee Code 1402	$500

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 45,215	Telephone 480.715.3895
Name (Print/Type)	Stuart A. Whittington		Date April 14, 2006

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

RECEIVED
CENTRAL FAX CENTER

APR 14 2006

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING FACSIMILE TRANSMITTED TO THE U.S. PATENT AND TRADEMARK OFFICE (FAX NO. (571) 273-8300) ON THE DATE INDICATED BELOW:

Date of Transmission: April 14, 2006 By: Stuart Whittington

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Eugene Matter et al. Atty. Docket No: 042390.P12396

Appln. No.: 10/003,170 Group Art Unit: 2187

Filed: November 14, 2001 Examiner: Mclean-Mayo, Kimberly

Title: MEMORY ADAPTED TO PROVIDE DEDICATED AND OR SHARED MEMORY TO MULTIPLE PROCESSORS AND METHOD THEREFOR

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF ON APPEAL

Pursuant to Appellant's Petition for Revival of an Unintentionally Abandoned Application and Notice of Appeal filed on February 15, 2006, Appellant presents this Brief in appeal of the Final Rejection dated July 22, 2005.

I. REAL PARTY IN INTEREST.

Intel Corporation is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES.

There are no related appeals or interferences before the Board of Patent Appeals and Interferences or related judicial proceedings known to Appellant, the Appellant's legal representatives, or assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

04/18/2006 EFLORES 00000083 500221 10003170

01 FC:1402 500.00 DA

III. STATUS OF CLAIMS.

Claims 1-34 have at one time, been pending in the present application. Claims 2, 5, 11, 13-15 and 22-34 were cancelled and thus only claims 1, 3-4, 6-10, 12 and 16-21 remain pending. Claims claims 1, 3-4, 6-10, 12 and 16-21 stand finally rejected and are the claims subject to this appeal, which are reproduced in attached Appendix A.

IV. STATUS OF AMENDMENTS.

No amendments to the application have been presented since the final rejection dated July 22, 2005. A response requesting reconsideration of the final rejections was submitted on October 24, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER.

Embodiments of the instant invention relate to multi-processor systems which utilize shared memory. (Specification, pg. 2, ll. 5-18). In certain embodiments, referring to Fig. 1, a portable computing or communication device 50 may include two or more processors 70, 80 and a memory device 30 such as a static random access memory (SRAM), dynamic RAM, a read only memory (ROM), an electrically erasable and programmable ROM or a flash memory, that may include a memory array 35. (Specification pg. 4, ll. 14 to pg. 5, ll. 1-10). Memory array 35 may be divided up or allocated such that portions 31-33 are dedicated to processors 70 and 80. For example, a first memory portion 33 may be only be accessible by processor 70 and a second memory portion 31 may only be accessible by processor 80. In addition, in certain

embodiments, a third memory portion 32 may be included and accessible by either one or both processors 70, 80. (Specification pg. 5, ll. 11-21). Memory portions 31-33 may share the signal (e.g., clock, sense amp) or power supply lines used in the operation of memory device 30. In certain embodiments, memory device 30 may be a dual-port memory having ports 37, 38 connected to respective first and second buses 75, 85. (Spec. pg. 6, ll. 17-20). In other embodiments, shared buses 290, 360, memory controllers 210, arbitrators 310 or other elements may be included to effect proper addressing and dynamic usage.

Memory array portions 31 and 33 may be divided to store data and/or instructions associated with various applications or processing requirements for each processor 70, 80. The third memory portion (e.g., 32, 232, 332) may be used to store data or instructions which may be needed by both processors 70 and 80. In one embodiment, during operation, portable communication device 50 may alter the respective size of memory portions 31, 32 and/or 33 in array 35 to accommodate operational needs of either or both processors 70 or 80. (Spec. pg. 7, ll. 11-13).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL.

The issues for consideration on this Appeal are:

A. Whether claims 1, 4, 6, 9-10, 16, 18-19 and 21 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over US 5,140,681 to Uchiyama et al. ("Uchiyama") in view of US 6,493,800 to Blumrich?

B. Whether claims 7-8, 12 and 20 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over US 5,140,681 to Uchiyama in view of US 6,493,800 to Blumrich in further view of US Application 22022/0184445 U.S. to Cherabuddi?

C. Whether claims 3 and 17 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over US 5,140,681 to Uchiyama in view of US 6,493,800 to Blumrich in further view of US 4,930,066 to Yokota?

VII. ARGUMENT.

A. APPELLANT'S CLAIMS ARE NOT RENDERED UNPATENTABLE BY THE COMBINATION OF UCHIYAMA IN VIEW OF BLUMRICH.

LEGAL STANDARD

It is well established that *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144).

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary sill in the art. *In re Kotzab*, 217 F.3d 1365,

1370 (Fed. Cir. 2000). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990).

ARGUMENT

All rejections set for the in the 7/22/05 Final Office Action rely on the main memory 5 of Uchiyama to be modified with Blumrich's dymamic partitioning of a cache memory. Appellant respectfully submits the present rejections are improper because (1) there is no proper motivation to combine these references as proposed; and (2) even when combining the teachings of Uchiyama with Blumrich, the limitations present in Appellant's independent claims are not disclosed or suggested.

(1) THERE IS NO PROPER MOTIVATION TO COMBINE REFERENCES

Uchiyama relates to subdividing a main memory 5 (see Figs. 2 and 5) into a shared region. Uchiyama main memory 5 is subdivided into a shared region to be subjected to a write access from a plurality of processors. Main memory 5 includes a copy-back region 61 dedicated to processor 1, a copy-back region 62 dedicated to processor 2 and shared write-through regions 60 and 63 which may be written to by either processor 1 or 2. (Col. 5, ll 15-28). Processors 1 and 2 have caches 3 and 4 (Fig. 2) respectively associate therewith, which are in turn connected to a main memory bus 7 so as to be linked to main memory 5. (Col. 3, ll. 46-51). Cashes 3 and 4 include address and data arrays 10-13 which are used to temporarily store data of main memory 5. (Col. 3, ll. 62-65).

Blumrich discloses a dynamically partitioned cache memory 70 (Fig. 7) which is shared among a plurality of entities (e.g., processors). Blumrich teaches that because caches are comprised of small amount of fast storage, they are expensive and it is advantageous to share. (Col. 1, ll. 47-49). However, independently operating processors can generate the same addresses which may actually refer to different memory locations. This may result in destructive collision in a shared cache. (Col. 2, ll. 5-12). Further, because processors frequently use different amounts of cache and a minimum amount may be required for a processor to achieve desired performance, Blumrich discloses a system that includes a cache segregator and a specially addressing format to dynamically vary the amount a cache that may be reserved for each processor.

The Office Action alleges it would be obvious to adapt Uchiyama main memory 5 to have the dynamic adjustment characteristics disclosed by Blumrich to provide "improved performance by providing efficient memory usage based on operating conditions of the system." Respectfully, Appellant notes that Uchiyama has its own cache system 12, 13 (Fig. 2). Further, there is no disclosure by Blumrich which would indicate or suggest that modification of a main memory (e.g., Uchiyama memory 5) to by dynamically partitionable would have any advantages or benefits whatsoever. Based on the addressing technique disclosed by Uchiyama, it is inferred that portions of main memory 5 are of a fixed size and thus Uchiyama certainly does not provide any motivation for dynamically altering the size of copy-back regions 61 and 62.

Respectfully, the motivation to modify the Uchiyama main memory partitions with the dynamic cache partitioning disclosed by Blumrich do not appear to be derived from the references themselves. Instead, it appears the motivation to combine references (i.e., to provide "improved performance by providing efficient memory usage based on operating conditions of the system") is merely conclusory and unsupported speculation by the Examiner.

In the absence of articulating an objective motivation, suggestion or teaching that would have lead the skilled artisan at the time of the invention to the claimed combination as a whole, it must be inferred that the motivation to combine the references is based on improper hindsight. *In re Rouffett*, 149 F.3d 1350, 1358 (Fed. Cir. 1998). Because the motivation to combine the cited references appears to be nothing more than a piecemeal attempt to reconstruct Appellant's claims using impermissible hindsight of Appellant's disclosure, Appellant respectfully submits that *prima facie* obviousness has not been established.

(2) THE PROPOSED COMBINATION OF UCHIYAMA AND BLUMRICH FAILS TO TEACH OR SUGGEST THE LIMITATIONS OF APPELLANT'S CLAIMS

Even assuming it would be proper to combine the teachings of Uchiyama with Blumrich as set forth in the Office Action (*arguendo*), Appellant respectfully submits that the resulting combination still fails to teach or suggest the limitations present in Appellant's claims. For example, claim 1 recites:

> *An apparatus comprising:*
> *an individual memory device including a memory array having a first portion and a second portion, the first portion of the memory array being different than the second portion of the memory array, wherein the memory array is adapted such that the first portion of the memory array is accessible only by a*

first processor and the second portion of the memory array is accessible only by a second processor, wherein the memory array further comprises a third portion that is different than the first portion and the second portion, the third portion of the memory array accessible by both the first processor and the second processor, and wherein the memory array is further adapted to dynamically alter a size of the first portion and the second portion of the memory array depending on an operational load of the first processor or the second processor.

Even when combining the teachings of Uchiyama with those of Blumrich, Appellant respectfully submits that the resulting combination would merely be a system having the fixed partitioned main memory 5 of Uchiyama and a cache memory 3, 4 that may be shared and dynamically adjusted as disclosed by Blumrich. In other words, the skilled artisan considering the teachings of Blumrich, would not modify the Uchiyama main memory 5 as alleged in the Office Action. Rather, based on the teachings of Blumrich, the skilled artisan would only consider dynamically partitioning and sharing the cache architecture/layout of Uchiyama caches 3, 4, as opposed to its main memory 5. It is only because Uchiyama main memory 5 shows separate portions which are convenient to compare to Appellant's claims for purposes of forming a rejection, that the Office Action alleges it would be obvious to modify Uchiyama main memory 5 with the dynamic cache allocation techniques disclosed by Blumrich.

Accordingly, even when combining Uchiyama and Blumrich, the resultant combination would not disclose or suggest an individual memory device including a memory array having first and second processor-exclusive portions which may be dynamically adjusted and a third shared portion accessible by both processors as recited in Appellant's independent claim 1 or dependent claim 18.

With respect to Appellant's independent claim 10, Appellant respectfully submits that Uchiyama teaches away from Appellant's claim limitations which recite *the first portion of the memory array is directly accessible only by the first processor via a first bus and the second portion of the memory array is directly accessible only by the second processor via a second bus*. Referring to Fig. 2 of Uchiyama, processors 1 and 2 have respective caches 3 and 4 which are connected to main memory 5 via a shared main memory bus 7 as opposed to first and second buses. (Col. 3, ll. 48-52). Furthermore, Blumrich does not disclose or suggest any type of bus architecture.

Because Uchiyama and Blumrich, taken alone or in combination, fail to teach or suggest at least the foregoing limitations of Appellant's claims, *prima facie* obviousness has not been established with respect to any of Appellant's claims based on the combination of Uchiyama and Blumrich. Accordingly, Appellant respectfully requests that the Board overturn the §103 rejection based on the combination of Uchiyama and Blumrich.

B-C. APPELLANT'S CLAIMS ARE NOT RENDERED UNPATENTABLE BY THE COMBINATION OF UCHIYAMA IN VIEW OF BLUMRICH IN FURTHER VIEW OF CHERABUDDI OR YAKOTA.

The secondary references Cherabuddi and Yakota are cited to address additional limitations present in Applellant's claims 7-8, 12 and 20 (Cherabuddi) and claims 3 and 17 (Yakota), for which the combination of Uchiyama and Blumrich alone admittedly fails to teach or suggest. Appellant does not address the properness of combining or the resultant combination of these additional secondary references and respectfully submits that a *prima facie* case of

obviousness has not been established with regard to either of the rejections relying on Cherabuddi or Yakota since these references fail to remedy the deficiencies of the proposed combination of Uchiyama and Blumrich described previously with respect to Applicant's independent claims 1 and 10. Namely, since there is no proper motivation for combining Uchiyama and Blumrich in the first place, and because even when combining Uchiyama and Blumrich several of Appellant's limitations are not disclosed or suggested, which neither Cherabuddi nor Yakota remedy and in many cases teach away from, *prima facie* obviousness has not been established with respect to any of Appellant's claims.

Since Uchiyama, Blumrich, Cherabuddi and/or Yakota, taken alone or in any combination, fail to disclose or suggest all the elements of Appellant's claims, the §103 rejections in the Final Office Action of 7/22/05 are believed to be improper and Appellant respectfully requests the Board is to overturn these rejections.

VIII. CONCLUSION.

It is respectfully submitted that in view of the foregoing all of the pending claims are patentable over the cited prior art references, alone or in any combination, and the Board is respectfully requested to overturn the rejections of record and allow this application to issue.

Respectfully submitted,

Stuart A. Whittington
Appellant's Attorney
Registration No. 45,215
Intel Corporation

(480) 715-3895

c/o
Blakely, Sokoloff, Taylor & Zafman, LLP
12400 Wilshire Blvd., Seventh Floor
Los Angeles, CA. 90025-1026
(503) 264-0967

Date: April 14, 2006

APPENDIX A
(Claims on Appeal)

1. (Previously presented) An apparatus comprising:

an individual memory device including a memory array having a first portion and a second portion, the first portion of the memory array being different than the second portion of the memory array, wherein the memory array is adapted such that the first portion of the memory array is accessible only by a first processor and the second portion of the memory array is accessible only by a second processor, wherein the memory array further comprises a third portion that is different than the first portion and the second portion, the third portion of the memory array accessible by both the first processor and the second processor, and wherein the memory array is further adapted to dynamically alter a size of the first portion and the second portion of the memory array depending on an operational load of the first processor or the second processor.

2. (Cancelled)

3. (Original) The apparatus of claim 1, wherein the first portion and the second portion of the memory array are both coupled to a same clock signal.

4. (Original) The apparatus of claim 3, wherein the first portion and the second portion of the memory array are coupled to a same power supply potential.

5. (Cancelled)

6. (Previously presented) The apparatus of claim 1, wherein the memory array is further adapted to increase the size of the first portion and decrease the size of the second portion due to an increase in the operational load of the first processor.

7. (Original) The apparatus of claim 1, wherein the memory array is further adapted such that the first processor may access the first portion of the memory array

APPENDIX A
(Claims on Appeal)

substantially simultaneously as the second processor accesses the second portion of the memory array.

8. (Original) The apparatus of claim 1, wherein the memory array is further adapted such that the first processor may read the first portion of the memory array as the second processor writes to the second portion of the memory array.

9. (Original) The apparatus of claim 1, wherein the memory array comprises memory selected from the group consisting of static random access memory, dynamic random access memory, read only memory, electrically erasable and programmable read only memory, and flash memory.

10. (Previously presented) An apparatus comprising:

an individual memory device including a memory array having a first portion and a second portion;

a first processor; and

a second processor, wherein the first portion of the memory array is directly accessible only by the first processor via a first bus, and the second portion of the memory array is directly accessible only by the second processor via a second bus.

11. (Cancelled).

12. (Original) The apparatus of claim 10, wherein the memory array comprises a first port and a second port, the first port coupling the first portion of the memory array to the first processor and the second port coupling the second portion of the memory array to the second processor.

13-15. (Cancelled)

APPENDIX A
(Claims on Appeal)

16. (Original) The apparatus of claim 10, wherein the memory array comprises a third portion that is different than the first portion and the second portion, wherein the third portion of the memory array is accessible by both the first processor and the second processor.

17. (Original) The apparatus of claim 10, wherein the first portion and the second portion of the memory array are both coupled to a same clock signal and a same power supply potential.

18. (Original) The apparatus of claim 10, wherein the memory array is adapted to dynamically alter a size of the first portion and the second portion of the memory array depending on an operational load of the first processor or the second processor.

19. (Original) The apparatus of claim 10, wherein the memory array is adapted to dynamically alter a size of the first portion and the second portion of the memory array depending on an operational load of the first processor and the second processor.

20. (Original) The apparatus of claim 10, wherein the memory array is further adapted such that the first processor may access the first portion of the memory array substantially simultaneously as the second processor accesses the second portion of the memory array.

21. (Original) The apparatus of claim 10, wherein the memory array comprises static random access memory.

22-34. (Cancelled)

APPENDIX B
(Evidence Appendix)

There is no additional evidence relied upon in this Appeal.

APPENDIX C
(Related Proceedings Appendix)

There are no proceedings or decisions related to this Appeal.